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• Cortex-A9 Floating-Point Unit Technical Reference Manual (ARM DDI 0408) • Cortex-A9 NEON™ Media Processing Engine Technical Reference Manual (ARM DDI 0409) • Cortex-A9 MBIST Technical Reference Manual (ARM DDI 0414) • Cortex-A9 Configuration and Sign-Off Guide (ARM DII 0146) • AMBA® AXI Protocol Specification (ARM IHI 0022 ...

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AM437x and AMIC120 ARM® Cortex™-A9 Processors Technical Reference Manual (Rev. I) Dec. 23, 2019: Application note: Ethernet PHY Configuration Using MDIO for Industrial Applications (Rev. A) May 07, 2021: White paper: Time sensitive networking for industrial automation (Rev. B) Jan. 20, 2021: More literature

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Sitara processor: Arm Cortex-A9, PRU-ICSS, EtherCAT, 3D graphics. Data sheet. AM437x Sitara™ Processors datasheet (Rev. E) I. Online data sheet. User guides. AM437x and AMIC120 ARM® Cortex™-A9 Processors Technical Reference Manual (Rev. I) Errata.

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Cortex A9 Technical Reference Cortex-A9 Technical Reference Manual. Other key resources. Cortex-A Series Programmer's Guide for Armv7-A Development tools for Cortex-A. Specifications. The Cortex-A9 processor is a performance and power optimized multi-core processor and it is one of Arm's most widely deployed and mature applications processors.

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ARM Cortex-A9 Technical Reference Manual has some explanation about "Exclusive L2 Cache": 8.1.5. Exclusive L2 cache The Cortex-A9 processor can be connected to an L2 cache that supports an exclusive cache mode. This mode must be activated both in the Cortex-A9 processor and in the L2 cache controller.

[arm - Performance of Cortex-A9 Exclusive L2 Cache Setting ...](#)

The Cortex-A9 MPCore documentation is summarized in the Technical Reference Manual (TRM). Technical Reference Manual The TRM describes the functionality and the effects of functional options on the behavior of the

[ARM® Cortex®?A9 MPCore Technical Reference Manual](#)

The prohibited regions are described in the ARM Architecture Reference Manual. The Cortex-A9 processor must determine prohibited regions for non-invasive debug in regions, including trace, performance monitoring, and PC sampling. Page 29 Functional Description Note Only entry to and exit from Jazelle state are traced.

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ARM CORTEX A9 MPCORE TECHNICAL REFERENCE MANUAL ULENHBXHSZ ULENHBXHSZ | PDF | 95 Pages | ARM CORTEX A9. f For further information about Cortex-A9 MPCore configurable options, refer to the. Introduction chapter of the Cortex-A9 MPCore Technical Reference Manual. .

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[AR# 47921: Zynq-7000 SoC - Processing System IP and...](#)

That is probably representative of most Cortex-A9 based systems. I think what the person intended by "L3 memory" was "the memory system". Furthermore I would like to know what type of interconnect are these connection AXI3 or AXI4? Cortex-A9 implements AMBA 3 AXI: Cortex-A9 MPCore Technical Reference Manual: 1.2.2.

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